## R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Mai for the indication of allowable matter.

## SUPPORT FOR CLAIM AMENDMENTS

Support for the amendment to the claims can be found in the drawings as originally filed, for example, on FIGS. 3-7 and in the specification as originally filed, for example, page 11, line 1 through page 12, line 15, on page 15, lines 1-10, and on page 20, line 14 through page 21, line 21. As such, no new matter has been introduced.

## CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 29 and 30 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement is respectfully traversed and should be withdrawn.

Contrary to the position taken by the Examiner on page 2, section 3 of the Office Action, one skilled in the art would clearly recognize in the instant specification a description of the invention defined by claims 29 and 30. Specifically, the claim language of claims 29 and 30 is supported by the drawings as originally filed (e.g., FIG. 3) and the specification as originally filed, for example, on page 11, line 17 through page 12, line 15.

In particular, one skilled in the art would recognize the control signals REF0-REF3 in FIG. 3 as examples of one or more control signals that may be used to control background operations in the memory array 104. Furthermore, one skilled in the art would recognize that the signals REF0-REF3 are generated in response to an address signal. Specifically, one skilled in the art would recognize that the signals REF0-REF3 are generated in response to the signal REF_BLK[0-3] (e.g., FIG. 6 of the specification). One skilled in the art would clearly understand from the specification that the signal REF_BLK[0-3] may be implemented as a decoded refresh block **address** (see page 12, lines 5-15 of the specification). Furthermore, one skilled in the art would understand based upon the specification as originally filed that the signal REF_BLK[0-3] is programmable, as presently claimed.

Specifically, one skilled in the art would recognize that the signal REF_BLK[0-3] may be presented by a refresh address register 138 as illustrated in FIG. 3 of the specification. One skilled in the art would further recognize that the register 138 is a programmable structure. In particular, the register 138 in FIG. 3 of the specification is described as being configured to latch the value of the signal AR1 in response to the signal LOAD. Therefore, the drawings, as originally filed, and the specification as originally filed, clearly provide a written description that would be recognized by one of ordinary skill in the art as

providing support for the address signal being programmable, as presently claimed. As such, claims 29 and 30 are fully patentable under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn.

## CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 5-8, 10-19 and 21-26 under 35 U.S.C. §102(b) as being anticipated by Arimoto (U.S. Patent No. 5,798,976) is respectfully traversed and should be withdrawn.

Arimoto is directed to a semiconductor memory device with reduced current consumption in a data holding mode (Title).

In contrast, the presently claimed invention (claim 1) provides a method for reducing power consumption during background operations in a memory array with a plurality of sections comprising the step of controlling the background operations in each of the plurality of sections of the memory array in response to one or more control signals, where the background operations can be enabled simultaneously in two or more of the plurality of sections independently of any other section. Claims 10 and 11 include similar limitations.

Applicants' representative does not agree with the position taken in the Office Action that "Arimoto clearly describes one of four memory mats (equivalent to memory sections as claimed) set in a selected state which means they are enabled independently

as claimed" (see page 8, lines 12-15 of the Office Action). Specifically, Arimoto states that the array control circuit 12 can "select **only one of the memory mats** when the data holding mode is designated" (column 5, lines 53-56 of Arimoto; emphasis added). Assuming, *arguendo*, the data holding mode of Arimoto is similar to the presently claimed background operations, Arimoto does not disclose or suggest that background operations can be enabled in each of a plurality of sections **independently** of the other sections. In particular, since **only one of the memory mats of Arimoto can be selected** when in the data holding mode, it follows that once one of the memory mats is selected none of the other memory mats can also be selected. Since more than one memory mat cannot be selected at the same time, it follows that each of the memory mats of Arimoto cannot be enabled independently of the other memory mats. For example, whether memory mat MM#0 of Arimoto can be selected **depends** upon whether one of the other memory mats MM#1-MM#3 is selected. Thus, the memory mats of Arimoto are not enabled independently of each other.

However, in light of what appears to be a broad interpretation of the term "independently," and in order to materially advance the prosecution of the present application, claims 1, 10 and 11 have been amended to recite that background operations can be enabled simultaneously in two or more of the plurality of sections. Since the background operations, as

presently claimed, can be enabled in each of the plurality of sections independently of the other sections, it follows that the background operations can be enabled simultaneously in two or more of the plurality of sections (see page 20, line 14 through page 21, line 17 of the specification).

Assuming, *arguendo*, the data holding mode of Arimoto is similar to the presently claimed background operations, since Arimoto states that the array control circuit 12 can "select **only one of the memory mats** when the data holding mode is designated" (column 5, lines 53-56 of Arimoto; emphasis added), it follows that Arimoto does not disclose or suggest background operations that can be **enabled simultaneously in two or more of the plurality of sections independently of any other section**, as presently claimed. Therefore, Arimoto fails to disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, the use of a decoder as taught by Arimoto (see element 12 in FIG. 5 of Arimoto) to generate the memory mat selection signals precludes more than one memory mat being enabled at a given time. Therefore, since more than one memory mat as taught by Arimoto cannot be enabled at a given time, Arimoto does not disclose or suggest background operations that can be enabled

simultaneously in two or more of a plurality of sections independently of any other section, as presently claimed. Therefore, Arimoto does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

The amendment of claims 1, 10 and 11 to recite that background operations can be enabled simultaneously in two or more of the plurality of sections is supported by the drawings, as originally filed, for example, in FIG. 3, and in the specification, as originally filed, for example, on page 20, line 14 through page 21, line 17. Specifically, although the specification does not use the word "simultaneously," one of ordinary skill in the art would recognize that since the present invention may provide a capability to refresh, for example, one-fourth, one-half, three-fourths and/or all of a memory array space (see page 20, lines 17-20 of the specification), multiple sections can be enabled simultaneously, as presently claimed. Furthermore, the specification, as originally filed, states:

> For example, to refresh one-half of the memory array of a device with four sections, the refresh block register may be configured to assert the signals REF0 and REF1 **to activate** the periphery array circuits of **the sections 0 and 1 of the memory array**. However, other patterns of activated sections may be implemented accordingly to meet the design

> criteria of a particular application. By not activating the periphery array circuits of sections 2 and 3, the standby current of the device is generally reduced (page 21, lines 9-17 of the specification; emphasis added).

For the above reasons, claims 1, 10 and 11 are believed to be fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-9, 12-26 and 29-30 depend, either directly or indirectly, from claim 1 or claim 11 which are believed to be allowable. Claim 31, which was indicated as being allowable, has been rewritten in independent form and is believed to be in condition for allowance. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Robert M. Miller
Registration No. 42,892
24840 Harper Avenue, Suite 100
St. Clair Shores, MI 48080
(586) 498-0670

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